



EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS
<i>277</i>	1	6,255,166 B1	07/03/2001	Ogura et al.	—	—
	2	5,408,115	04/18/1995	Chang	—	—
	3	5,969,383	10/19/1999	Chang et al.	—	—
	4	5,422,504	06/06/1995	Chang et al.	—	—
	5	5,494,838	02/27/1996	Chang et al.	—	—
	6	6,177,318 B1	01/23/2001	Ogura et al.	—	—
	7	6,248,633 B1	06/19/2001	Ogura et al.	—	—
	8	US 2002-0100929 6,809,385	08/01/2002	Ebina et al.	—	—
	9	US 2003-0127605 6,709,922	09/12/2002	Ebina et al.	—	—
	10	6,413,821	07/02/2002	Ebina et al.	—	—
	11	6,518,124	02/11/2003	Ebina et al.	—	—
	12	US 2003-0054610 6,627,461	05/20/2003	Ebina et al.	—	—
	13	US 2003-0057505	03/27/2003	Ebina et al.	—	—
	14	US 2003-0058705 6,812,520	03/27/2003	Ebina et al.	—	—
	15	US 2003-0060011	03/27/2003	Ebina et al.	—	—
	16	US 2003-0190805 6,849,553	10/09/2003	Inoue	—	—
	17	US 2003-0186505 6,656,794	10/02/2003	Shibata	—	—
	18	US 2003-0166321 6,815,291	09/04/2003	Kasuya	—	—
	19	US 2003-0157767	08/21/2003	Kasuya	—	—
	20	US 2003-0166322 6,706,579	09/04/2003	Kasuya	—	—
	21	US 2003-0166320 6,664,155	09/04/2003	Kasuya	—	—
	22	US 2003-0211091 6,818,507	11/13/2003	Ueda	—	—
	23	10/636,562 US 2004-72402	08/08/2003	Inoue	—	—
	24	10/636,581 US 2004-97035	08/08/2003	Yamamukai	—	—
	25	10/636,582 US 2004-72403	08/08/2003	Inoue	—	—
	26	10/614,985 US 6,787,417	07/09/2003	Inoue	—	—
	27	10/689,993 US 2004-129972	10/22/2003	Kasuya	—	—
<i>277</i>	28	10/689,989 US 2004-135196	10/22/2003	Kasuya	—	—

Date: March 22, 2004

29	10/689,990	10/22/2003	Kasuya		
FOREIGN PATENT DOCUMENTS					
	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS
30	JP A 2001 156188 (with abstract and translation) <i>corresponds to US 6,335,534</i>	06/08/2001	Japan		
<i>RKH</i>	31 JP A 7-161851 (with abstract and translation)	06/23/1995	Japan		
<i>RKH</i>	32 JP B1 2978477 (with translation)	09/10/1999	Japan		
OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)					
<i>RKH</i>	33 Hayashi et al. "Twin MONOS Cell with Dual Control Gates", 2000 Symposium on VLSI Technology Digest of Technical Papers				
<i>RKH</i>	34 Chang et al. "A New SONOS Memory Using Source-Side Injection for Programming", IEEE Electron Device Letters, Vol. 19, No. 7, July 1998, pp 253-255				
<i>RKH</i>	35 Chen et al. "A Novel Flash Memory Device with S Plit Gate Source Side Injection and ONO Charge Storage Stack (SPIN), 1997 Symposium on VLSI Technology Digest of Technical Papers, pp 63-64				
EXAMINER <i>G. MUNSON</i>			DATE CONSIDERED <i>18 FEBRUARY 2005</i>		
Examiner: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.					

Date: March 22, 2004